

RANDOM ACCESS MEMORY HAVING AN ADAPTABLE LATENCY

Abstract of the Disclosure

A random access memory circuit comprises a plurality of memory cells and at least one decoder coupled to the memory cells, the decoder being configurable for receiving an input address and for accessing one or more of the memory cells in response thereto. The random access memory circuit further comprises a plurality of sense amplifiers operatively coupled to the memory cells, the sense amplifiers being configurable for determining a logical state of one or more of the memory cells. A controller coupled to at least a portion of the sense amplifiers is configurable for selectively operating in at least one of a first mode and a second mode. In the first mode of operation, the controller enables one of the sense amplifiers corresponding to the input address and disables the sense amplifiers not corresponding to the input address. In the second mode of operation, the controller enables substantially all of the sense amplifiers. The memory circuit advantageously provides an adaptable latency by controlling the mode of operation of the circuit.